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1 Plan

This document outlines the proposed PhD research plan for the forthcoming academic year, building upon the outcomes and insights gained during the preceding year.

1.1 Link to Previous PhD Plan

<https://github.com/Akilan1999/phd-thesis/releases/download/Year2/thesis.pdf>

1.2 Summary of the Previous Plan

1.2.1 Phase 1: FAT-Pointer Mechanism (JulySeptember 2024)

1. 1st15th July 2024

- Investigated causes of L1 TLB misses associated with contiguous memory allocation.
- Executed performance benchmarking using COZ on selected C programs.

- Ported the kernel module to support SnMalloc, the default allocator in CheriBSD.

2. 15th30th July 2024

- Conducted benchmarking using the SPEC and XSBench suites.
- Performed comparative analysis with both baseline and modified SnMalloc implementations.

3. August 2024

- Initiated drafting of a manuscript for submission to EuroSys, focusing on the FAT-Pointer memory allocator.

4. September 2024

- Compiled and structured thesis chapter related to the FAT-Pointer architecture.
- Finalised and submitted the EuroSys paper.

1.2.2 Phase 2: RISC-V Integration (October 2024 May 2025)

1. OctoberDecember 2024

- Modified the Bluespec implementation to enable TLB bypass in the memory access pipeline.
- Configured the experimental platform and evaluation toolchain.

2. JanuaryFebruary 2025

- Undertook experimental evaluation of the FAT-Pointer system on RISC-V (Toooba).
- Commenced drafting of a technical paper for ISMM based on RISC-V integration results.

3. MarchMay 2025

- Addressed outstanding tasks and technical backlog.
- Continued development of the corresponding thesis chapter.

1.2.3 Phase 3: Uni-Kernel Deployment (May 2025 – September 2026)

1. May–December 2025

- Ported the memory allocator to a CHERI-enabled Uni-Kernel environment.
- Designed and implemented a unified memory allocator to support both kernel and user-level allocations.
- Initiated drafting of a manuscript targeted at OSDI.

2. January–September 2026

- Finalised documentation and submission of the PhD thesis.
- Submitted third research paper based on extended evaluation.

1.3 Current Research Plan

1.3.1 June–July 2025

- Refactored BlueSpec SystemVerilog (BSV) modules within the CHERI Toooba architecture.
- Set up a bare-metal C benchmark suite for execution on the Bluespec simulation platform.
- Incorporated supervisory team feedback into revisions of the EuroSys paper.
- Undertook formal progression review requirements.
- Submitted EuroSys manuscript to the CHERI research team at the University of Glasgow for preliminary feedback.

1.3.2 July–August 2025

- Engaged in extensive debugging of the Toooba memory pipeline, specifically targeting the TLB bypass path.
- Finalised and validated the C benchmark suite for Toooba evaluation.
- Began technical documentation of the Toooba workflow, to support a second publication.
- Concluded revisions to the EuroSys paper by the end of July.

1.3.3 ~~August~~September 2025

- Continued debugging efforts within the Toooba memory subsystem.
- Drafted the abstract, introduction, and methodology sections of the second research paper.
- Aimed to generate preliminary experimental results for inclusion in the evaluation.

1.3.4 ~~September~~October 2025

- Published the EuroSys paper detailing the FAT-Pointer allocator.
- Commenced benchmarking of the Toooba design.
- Simultaneously drafted the evaluation and analysis sections of the second manuscript.

1.3.5 ~~October~~November 2025

- Initiated third experimental phase, aimed at deeper evaluation of prior experiments.
- Modified memory allocators (TcMalloc and Mesh) to remove reliance on ‘mmap’.

1.3.6 ~~November~~December 2025

- Stripped away huge-page-specific optimisations from JeMalloc, TcMalloc, and Mesh.
- Analysed instruction-level reductions and performance implications.
- Commenced drafting of the third research paper, building on contributions from the EuroSys paper.

1.3.7 December 2025 January 2026

- Conducted evaluation and profiling for the third paper.
- Commenced thesis chapter write-up for Experiments 1 and 2.

1.3.8 JanuarySeptember 2026

- Continued thesis development and refinement across all experimental chapters.
- Finalised and submitted third manuscript for peer review.
- Prepared complete PhD dissertation for submission.